The following is a complete listing of all claims in the application, with an indication of the status of each:

Listing of claims:

1. (Previously Presented) An instruction buffer comprising:

a sequence of instructions arranged in an order determined beforehand; and

a first buffer including entries arranged in a preselected entry number order for storing said sequence of instructions; and

a second buffer including other entries for storing instructions, wherein an instruction stored in any one of said other entries earlier than other instructions is issued earlier than said other instructions,

wherein any one instruction of said sequence of instructions stored in any one of the entries designated by a low relatively lower entry number is prior, in order, to another instruction stored in another entry designated by a high relatively higher entry number.

2. (Original) The instruction buffer as claimed in claim 1, wherein the entries each show whether or not the instruction stored therein is ready to be issued.

3. (Previously Presented) The instruction buffer as claimed in claim 2, wherein the instruction is first issued from among the entries whose instructions are ready to be issued is the entry having a lowest entry number among said entries whose instructions are ready to be issued.

4. (Original) The instruction buffer as claimed in claim 3, wherein the entries storing the instructions are lower in entry number than the entries storing no instructions.

5. (Cancelled)

6. (Previously Presented) A method of controlling a buffer queue, comprising the steps of:

generating a first group of instructions in an a priority order determined beforehand;

generating a second group of instructions belonging to said first group of instructions and capable of being executed; and

executing one instruction of said second group of instructions highest in priority order.

7. (Previously Presented) The method as claimed in claim 6, further comprising the steps of:

generating a third group of instructions included in said first group of instructions; and

generating a fourth group of instructions included in said first group of instructions and not dependent on said third group of instructions;

wherein when one of said fourth group of instructions highest in priority order does not belong to said second group of instructions, none no instruction of said fourth group of instructions is executed.

8. (Previously Presented) The method as claimed in claim 7, wherein one of preselected two instructions belonging to said third group or fourth group of instructions is not executable until the other instruction of said two instructions is executed.

9. (Original) The method as claimed in claim 8, wherein the instructions belonging to said third group are executed at the same time as the instructions belonging to said fourth group.

10. (Original) The method as claimed in claim 9, wherein the instructions belonging to said third group and the instructions belonging to said fourth group and operation instructions and memory access instructions, respectively.

11 (New). A buffer queue control comprising:

a reorder buffer for subsequently registering a plurality of instructions in an order of instruction:

a first buffer for storing first instructions included in the plurality of instructions;

a second buffer for storing, among the plurality of instructions, second instruction other than the first instructions;

said second instructions including an instruction that should be issued after first instruction;

said first buffer including a plurality of first entries for sequentially storing the first instructions in said order of instruction;

said buffer queue control further comprising the steps of:

releasing any one of the plurality of first entries that stores an instruction issued;

shifting any one of the first instructions that is not issued to an entry prior, in order, by one;

issuing one of the second instructions, which can be issued, earliest in said order of instruction; and

deleting any one of the plurality of instructions that has been executed and is earlier, in said order of instruction, than instruction not executed.

12 (New). The buffer queue control as claimed in claim 11 further comprising the step of issuing any one of the first instructions that is earliest in said order of instruction and ready to be issued.

13 (New). The buffer queue control as claimed in claim 12, wherein said second buffer comprises a plurality of second entries each for storing a particular one of the second instructions in said order of instruction, an issuance pointer for controlling issuance of said second instructions, and a head pointer indicative of an entry that has been issued last.

14 (New). The buffer queue control as claimed in claim 13, wherein one of first instructions can be executed at the same time as one of second instructions.

15 (New). The buffer queue control as claimed in claim 14, wherein the first instructions comprise operation instructions while the second instructions comprise memory access instructions.